

Applicant: Drapkin et al.
Application No.: 09/651,944

REMARKS

The present application contains claims 1-3, 5, 6, 8, 9, 12, 13, 18, 19, 23 and 25-27. Claims 1-3, 5, 8, 12, 13, 18, 19, 23, 26 and 27 have been amended. Claims 28-31 haven been newly added. Claims 20 and 22 have been canceled without prejudice to Applicant in order to expedite the prosecution of the present application.

Claims 1-3, 5, 6, 8, 9, 12, 13, 18-20, 22, 23 and 25-27 have been rejected under 35 U.S.C. §102(b) as anticipated by U.S. Patent No. 5,808,488 (Bruccoleri). This rejection is respectfully traversed regarding all of the above-mentioned claims except for claims 20 and 22 which have been canceled without prejudice to Applicant in order to expedite the prosecution of the present application.

The Examiner states that regarding claims 1, 2 and 18, 12 and 22, Bruccoleri in Figure 3 shows a method for reducing distortion of a signal to an input of an input/output device having parasitic capacitance, comprising the steps of: 1) detecting the direction of change of the input voltage of the input of inverter (INV1); and 2) introducing a current to the parasitic capacitance (Cin) when the output of inverter (INV2) becomes high level output when a positive edge of the input signal is applied to the input of inverter (INV1) to charge the parasitic capacitance (Cin) to compensate the current of the input signal charging said parasitic capacitance.

The Examiner states that when the input signal voltage rises and is still below the threshold voltage of the circuit input, the input parasitic capacitance (C_{in}) formed by the gate-source/drain of the transistor(s) of inverter (INV1) starts to be charged. When a rising edge of the input signal is detected to be higher than the input threshold, the output voltage of inverter (INV1) becomes low and the output of inverter (INV2) becomes high, and thus a current is introduced to the parasitic capacitor (C_{in}) to compensate for current of the input signal that charges the parasitic capacitor (C_{in}). The Examiner further notes that the parasitic capacitance (C_{in}) exists across the input and ground.

Making reference to Figure 3 of Brucolieri, it should be noted that detection of a change of current at the input to INV1 appears at the INV1 output and is applied from the output thereof to the input of INV2, whose output couples the current to the input of INV1.

It should be noted that the present invention teaches a technique wherein the change in current is detected directly at the input of the circuit. Brucolieri fails to teach or even remotely suggest such an arrangement. For example, in Figures 2A through 2C of the present application, it should be noted that the detection system 10 is directly coupled to the input of the circuit R. Independent claims 1 and 12 positively recite detecting directly at said circuit input, a direction of change of voltage of said input signal. Claim 12 is amended in a like fashion. Claims 2 and

Applicant: Drapkin et al.
Application No.: 09/651,944

18 depend from claim 1 and carry all of its limitations and hence are deemed to patentably distinguish over Brucolieri for the same reasons set forth hereinabove with respect to claim 1. Claim 22 has been canceled without prejudice and rejection of this claim is now moot.

The Examiner states that regarding to claims 3, 19, 13, 23 and 27, Brucolieri shows a method of reducing the distortion of a signal applied to the input of a circuit having a parasitic capacitance, the parasitic capacitance Cin discharging through inverter INV2 to prevent discharging a parasitic capacitance into the input signal.

In spite of this, it should be noted that the circuitry of Figure 3 directed to claims 3, 19, 13, 23 and 27 requires that the detection of a change of signal is obtained at the output of INV1, which is applied to the input of INV2 whose output is then coupled to the input of INV1.

Claim 3 has been amended to recite detecting directly at the input of said circuit a direction of change in a direction of change in voltage of said input signal. This feature is not found in Brucolieri and it is submitted that the claim 3 clearly patentably distinguishes over Brucolieri. Claim 19 depends from claim 3 and carries all of its limitations and hence is deemed to patentably distinguish over Brucolieri for the same reasons set forth hereinabove with respect to claim 3.

Claim 13 has been amended in like fashion, reciting detecting directly at said input a direction of change in voltage of said input signal. This feature is neither

Applicant: Drapkin et al.
Application No.: 09/651,944

taught nor remotely suggested by Brucolieri and it is submitted that claim 13 patentably distinguishes thereover. Claim 23 depends from claim 13 and carries all of its limitations and hence is deemed to patentably distinguish over Brucolieri for the same reasons as set forth hereinabove with respect to claim 13.

Claim 27 has similarly been amended to recite detecting directly at said input a direction of change in voltage of said input signal and hence is deemed to patentably distinguish over Brucolieri for this reason.

The Examiner states that, with regard to claims 5, 6 and 25, Brucolieri shows an apparatus in Figure 3 for introducing current to the parasitic capacitance C_{in} to compensate for current of the input signal that charges C_{in} .

Apparatus claim 5 has been amended to recite a detection circuit directly coupled to said input for detecting a change in voltage of said input signal coupled to said input and a correction circuit coupled between said detection circuit and said input for compensating for current from said input signal diverted to said parasitic capacitance due to a positive edge of said input signal. These features are neither taught nor remotely suggested by Brucolieri and it is submitted that claim 5 patentably distinguishes thereover.

Claim 6 depends from claim 5 and carries all of its limitations and hence is deemed to patentably distinguish over Brucolieri for the same reasons as set forth hereinabove with regard to claim 5.

Applicant: Drapkin et al.
Application No.: 09/651,944

Claim 25 depends from claim 6 and is deemed to patentably distinguish over Brucolieri for the same reason as set forth hereinabove with regard to claims 5 and 6.

The Examiner has relied upon Figure 3 of Brucolieri for the rejection of claims 8, 9 and 20 stating that the circuit of Figure 3 prevents the addition of current from the parasitic capacitance to be added to the input signal. Again it should be noted that independent apparatus claim 8 has been amended to recite the detection circuit as being directly coupled to said input for detecting a change in the voltage of input signal coupled to the input and a correction circuit coupled between the detection circuit and said input for compensating for said parasitic capacitance to be added to said input signal due to a negative edge of said input signal. These features are neither taught nor remotely suggested by Brucolieri and it is submitted that claim 8 patentably distinguishes thereover.

Claims 9 and 20 depend from claim 8 and carry all of its limitations and hence are deemed to patentably distinguish over the Brucolieri for the same reasons as set forth hereinabove with regard to claim 8.

Claims 1, 2, 5, 6, 12, 18, 22, 25 and 26 have been rejected under 35 U.S.C. §102(e) as anticipated by U.S. Patent No. 6,107,868 (Diniz). This rejection is respectfully traversed with regard to all of the above claims except for claim 22

Applicant: Drapkin et al.
Application No.: 09/651,944

which has been canceled without prejudice to Applicant in order to expedite the prosecution of the present application.

The Examiner states that regarding claims 1, 2, 18, 12, 22 and 26, Figure 3 of Diniz shows a method for reducing distortion of a signal to an input of an input/output device having parasitic capacitance comprising the steps of: 1) detecting a direction of change of the input; and 2) introducing a current 64 when the positive edge of the input signal is applied to the gate of transistor 48 to charge a parasitic capacitance, and inherently existing between the gate of and the source of transistor 48 to compensate the current of the input signal charging said parasitic capacitance.

It should be noted that current 64 is controlled by the signal appearing at the output (i.e., source electrode) 54 of transistor 48 which output is coupled to the gate of transistor 44, whose drain electrode is coupled to the input (i.e., gate) of transistor 48. As was pointed out hereinabove in response to the rejection of the claims based on Brucolieri, the change in the input signal in the present invention is detected directly at the input of the circuit. In Diniz, the increase in the signal applied to the input of transistor 48 must first appear at the output 54 and then be coupled to the gate of transistor 44 whose source is then coupled to the input or gate of transistor 48. This is a clearly different arrangement from that taught in the present invention and it is submitted that claims 1, 2, 5, 6, 12, 18, 25 and 26, all of

Applicant: Drapkin et al.
Application No.: 09/651,944

which have been discussed above as containing limitations, or which depend from claims which contain limitations, of the detection taking place directly at the input of the circuit, patentably distinguish over both Diniz and Brucolieri which detect changes in the input signal at the output (and not the input) of the "circuit."

New apparatus claim 28 depends from apparatus claim 5 discussed above and further recites that said circuit has an output and the detector circuit is isolated from said output.

Claim 29 depends from apparatus claim 8 and recites the same limitations as claim 28. It is clear from both the Diniz and Brucolieri that the detector circuits are not isolated from the output. Note that output 54 in Diniz is connected to the gate of transistor 44 whose drain electrode provides the current 64. Also note Figure 3 of Brucolieri in which the input of INV2 is directly coupled to the output of INV1 and not isolated therefrom. In view of the foregoing, it is submitted that claims 28 and 29 patentably distinguish over Diniz and Brucolieri for the same reasons as set forth hereinabove with regard to claims 5 and 8 and further for the limitations as set forth in claims 28 and 29 which are not found or even remotely suggested in either of Diniz or Brucolieri

Claim 30 depends from apparatus claim 5 further reciting that the detection circuit is independent of said first mentioned circuit (i.e., the circuit whose input has the drain electrode coupled across its input and ground. It should be noted that

Applicant: Drapkin et al.
Application No.: 09/651,944

Diniz has the detection circuit, i.e. transistor 44 directly coupled to the source of transistor 48 is not isolated therefrom.

New claim 31, which is dependent upon claim 8 recites the same limitations of claim 30 and it is submitted that claims 30 and 31 patentably distinguish over both the Diniz and Brucolieri.

In view of the foregoing, it is submitted that all of the claims remaining in the present application patentably distinguish over the art of record and reconsideration and allowance of these claims are earnestly solicited.

Favorable action is respectfully awaited.

Respectfully submitted,

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